## Amendments to the Specification:

Please replace paragraph [0004] with the following rewritten paragraph:

**[0004]** Further referring to Fig. 2, the transformation of the written-in signal X into the signal Y is illustrated. The written-in signal X, for example, consists of levels +0.5 and –0.5. Before the written-in signal X is transformed into the signal Y by the equalizer 14, it is processed into a signal Z first via a channel 20. The channel 20 substantially involves all factors that the written-in signal X encounters after it is read out from the digital data recording medium 10 and before it enters the equalizer 14. The transfer function of the channel 20 is defined as ~~"Z(D)/X(D)□1□a1□D□a2□D^2□a3□D^3□a4□D^4□…".~~ "Z(D)/X(D) = 1 + a1 * D + a2 * D^2 + a3 * D^3 + a4 * D^4 + …". On the other hand, the channel 20 and the equalizer 14 can be combined as a partial response (PR) channel with an input signal X and an output signal Y. Accordingly, the transfer function can be adjusted into ~~"Y(D)/X(D)□PR(1,1)□1□D", "Y(D)/X(D)□PR(1,2,1)□1□2□D□D^2" or "Y(D)/X(D)□PR(1,1,1,1)□1□D□D^2□D^3"~~ "Y(D)/X(D) = PR(1,1) = 1 + D", "Y(D)/X(D) = PR(1,2,1) = 1 + 2 * D + D^2" or "Y(D)/X(D) = PR(1,1,1,1) = 1 + D + D^2 + D^3". Table 1 lists the relationship between the transfer functions and their corresponding target levels, i.e. the ideal levels of the signal Y.

Table 1

| Transfer function Y(D)/X(D) | Target levels |
|---|---|
| ~~PR(1,1)□1□D~~ PR(1,1) = 1 + D | -1, 0, 1 |
| ~~PR(1,2,1)□1□2□D□D^2~~ | -2, -1, 1, 2 |
| PR(1,2,1) = 1 + 2*D + D^2 | |
| ~~PR(1,1,1,1)□1□D□D^2□D^3~~ | -2, -1, 0, 1, 2 |
| PR(1,1,1,1) = 1 + D + D^2 + D^3 | |

Please replace paragraph [0031] with the following rewritten paragraph:

**[0031]** The present invention is now described in more detail as follows. The ~~EMCU~~ BMCU 51 receives the consecutive data y(k-n), ..., y(k-1), y(k), and then performs branch metric calculating operations of the consecutive data y(k-n), ..., y(k-1), y(k) according to a plurality target level sets. That is, the differences of the input data with all the corresponding target values are squared to obtain a plurality of branch metric values. For example, it is assumed two consecutive data y(k) and y(k-1) are inputted to the ~~EMCU~~ BMCU 51, and two target level sets (2,1,0,-1,-2) and (1.5,1,0,-1,-1.5) are provided in the partial response channel PR(1,1,1,1). Then, branch metric values (y(k)-2)^2, (y(k)-1)^2, (y(k))^2, (y(k)+1)^2, (y(k)+2)^2, (y(k-1)-1.5)^2, (y(k-1)-1)^2, (y(k-1))^2, (y(k-1)+1)^2, (y(k-1)+1.5)^2 are obtained, as shown in Fig. 7. The target levels vary with the partial response channel of the system. For example, the above target levels are based on PR(1,1,1,1), and the derivation of the target levels will be described hereinafter.

Please replace paragraph [0033] with the following rewritten paragraph:

**[0033]** Further referring to Fig. 7 again, the consecutive data y(k) and y(k-1) and the corresponding target level sets (2,1,0,-1,-2) and (1.5,1,0,-1,-1.5) perform respective branch metric calculation operation in the ~~EMCU~~ BMCU 51 to output the branch metric values (y(k)-2)^2, (y(k)-1)^2, (y(k))^2, (y(k)+1)^2, (y(k)+2)^2, (y(k-1)-1.5)^2, (y(k-1)-1)^2, (y(k-1))^2, (y(k-1)+1)^2, (y(k-1)+1.5)^2 to the adder-comparator-selector unit 52. The adder-comparator-selector unit 52 includes a plurality of accumulators 521, a plurality of comparators including comparators 5221 and 5222, a plurality of selectors 5231 and 5232. In this embodiment, eight accumulators 521 corresponding to the eight possible output-data state transition tracks illustrated with reference to Fig. 6A are provided. The inputs (y(k)+2)^2, (y(k-1)+1.5)^2 and fed-back value stored in a register 541 of the metric register unit 54 are added by the first accumulator 5211, and the resulting value indicates a branch metric accumulation value in response to the change from 00 to 00. Likewise, the accumulated value obtained by the second accumulator 5212 indicates a branch metric accumulation value in response to the change from

01 to 00, and the accumulated value obtained by the third accumulator 5213 indicates a branch metric accumulation value in response to the change from 11 to 00. The accumulated values are compared in the comparator 5221, and a two-bit first control signal C1 is outputted according to the comparing result. In response to the control signal C1, the selector 5231 selects the least one of the accumulated values outputted by the accumulators 5211, 5212 and 5213 to be outputted to the register 541 to be stored, and the stored value of the register 541 is fed back to corresponding accumulators of the adder-comparator-selector unit 52 for next accumulation operations. In addition, the accumulated values obtained by the other accumulators indicate branch metric accumulation values in response to the changes from 11 to 01, from 00 to 10, and from 00, 10 or 11 to 11. Likewise, the second comparator 5222 receives and compares associated branch metric accumulation values, and outputs a two-bit second control signals C2 according to the comparing result. The second selector 5232 then outputs the least accumulated values to the register 544 of the metric register unit 54 to be stored. The stored value in the register 544 is fed back to corresponding accumulators of the adder-comparator-selector unit 52 for next accumulation operations. On the other hands, the registers 542 and 543 of the metric register unit 54 receive and store accumulated values directly since no comparison and selection operations are required. The stored values of the register 542 and 543 are also fed back to corresponding accumulators of the adder-comparator-selector unit 52 for next accumulation operations.